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Applicant: Andrew J. Burstein et al.

Serial No.: 09/892,233

: June 26, 2001

TECHNOLUG: Examiner UC Unknown

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Attorney's Docket No.: 09464-009

Filed Title

TRANSISTOR PATTERN FOR VOLTAGE REGULATOR

Commissioner for Patents Washington, D.C. 20231

## **INFORMATION DISCLOSURE STATEMENT**

Applicant submits the references listed on the attached form PTO-1449.

Under 35 USC §120, this application relies on the earlier filing date of application serial number 09/498,297, filed on February 4, 2000. References AA-AD listed on the attached form PTO-1449 were submitted to and/or cited by the Patent Office in the prior application and, copies therefore, are not provided in this application.

This statement is being filed within three months of the filing date of the application or before the receipt of a first Office action on the merits. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date:

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## CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

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